REMARKS

Claims 27-51 are currently pending. Claim 27 is an independent claim. All of the remaining pending claims depend, either directly or indirectly, on claim 27.

The Office Action rejected all of the pending claims. At least for the reasons articulated below, the Applicant respectfully submits that the Office Action does not set forth a proper prima facie rejection and, therefore, the claims are allowable over the cited art.

The Office Action rejected claims 27-51 under 35 U.S.C. § 103 as unpatentable over the combination of U.S. Patent No. 6,175,279 to Ciccarelli et al. ("Ciccarelli"), U.S. Patent No. 6,445,170 to Pangal et al. ("Pangal"), and U.S. Patent No. 6,275,090 to Burger, Jr. et al. ("Burger"). The Applicant respectfully submits that Pangal and Burger lack some of the limitations present in independent claim 27 and, by implication, in all of the pending claims.

More specifically, claim 27 recites (emphasis added):

> 27. A radio-frequency (RF) apparatus, comprising:
> a first integrated circuit, including:
> a reference current generator configured to generate a
> reference output current, the reference current
> generator comprising:
> a reference voltage source configured to provide
> a reference voltage;
> a controllable current source configured to
> provide the reference output current in
> response to a first plurality of signals;
> and
> a first controller configured to provide the first
> plurality of signals, the first plurality of
> signals being derived from the reference
> voltage and the reference output current,
> *wherein a noise content of the reference output
> current is lower than a noise content of
> the reference voltage.*

The Applicant respectfully submits that neither Pangal nor Burger teaches or suggests the highlighted language of claim 27.

Citing Pangal, the Office Action asserts that Pangal teaches that "a noise content of the reference output current is *inherently* lower than a noise content of the reference voltage (See fig. 6 and col. 6 line 51 to col. 7 line 35)." Office Action at 3 (emphasis added). The Applicant respectfully disagrees.

The passage of Pangal that the Office Action cites provides in its totality:

> FIG. 6 shows an integrated circuit having a current reference and a control loop circuit. Integrated circuit 600 includes two current references 602 and 608, voltage reference 106, voltage comparator 604, and state machine 606. Current reference 602 is shown as current reference 300 (FIG. 3) with voltage reference 106 being shared between current references 602 and 608. Each of variable resistors 302, 310, and 306 within current reference 602 are driven by control signals generated by state machine 606 on nodes 612 and 614. Current reference 602, voltage comparator 604, and state machine 606 form a control loop circuit that modifies the resistance values of variable resistors 302, 306, and 310. Also shown in FIG. 6 is resistor 630, which is external to integrated circuit 600. High precision resistors are readily available, and resistor 630 can be a high precision resistor selected for a particular application of integrated circuit 600.
>
> Current source 602 generates an output current on node 610 as described with reference to the previous figures. This current travels through precision resistor 630 and generates a voltage. This voltage is compared against the reference voltage by voltage comparator 604. In some embodiments, voltage comparator 604 produces a digital output on nodes 605, which is input to state machine 606. In some embodiments, state machine 606 includes a counter that counts up or down depending on the value of the digital signal on nodes 605. As state machine 606 counts up or down, control signals on nodes 612 and 614 modify resistance values of variable resistors 304, 302, and 306. As a result of the change in resistance values, current reference 602 modifies the current on output node 610, and the loop is closed.
>
> By utilizing variable resistors 302, 310, and 306, resistance values

can be trimmed to match, or to be a function of, the resistance of an external precision resistor. When the control loop circuit is locked and the variable resistors internal to current reference 602 have stable resistance values, the output current on output node 610 satisfies equation (7), above, where "R" is the static value of variable resistors 302 and 306.

Integrated circuit 600 includes two current references 602 and 608. The output current from current reference 602 is utilized to close the control loop that generates control signals on nodes 612 and 614. Current reference 608 receives the control signals on nodes 612 and 614 and produces a current reference output current (shown as "I_{REF}" in FIG. 6) on node 620.

Any number of current references can utilize the control signals on nodes 612 and 614. One current reference, current reference 602, is used to close the control loop circuit, but many more current references can utilize control signals generated thereby.

Pangal at col. 6, line 51 to col. 7, line 35. The passage does not discuss a noise content of a reference output current and its relative value to a noise content of a reference voltage. Nothing in the passage appears to relate to relative noise values, inherently or otherwise. In fact, the word "noise" does not appear in that passage or any other part of Pangal. Thus, the Applicant respectfully submits that the Office Action improperly asserts that "a noise content of the reference output current is inherently lower than a noise content of the reference voltage." If the Office still believes that relative noise values are somehow inherent in Pangal's teachings, the Applicant respectfully requests that the Office provide concrete evidence to that effect (e.g., an Examiner's declaration).

Similarly, citing Burger, the Office Action asserts that it teaches that "a noise content of the reference output voltage is *inherently* lower than a noise content of the reference voltage (See fig. 1 and col. 2 lines 8-42)." Office Action at 4 (emphasis added). The Applicant respectfully disagrees.

The cited passage in Burger provides in its entirety:

The following detailed description relates to a technique for implementing a self-calibrating resistor on an integrated circuit. Referring to FIG. 1, an illustrative embodiment of the invention is shown. A reference current source 101 provides a reference current I_{REF} that flow through a series string of calibration resistors 103, 104, 105 and 106. Node 102 at the top of the string is connected to the inverting input of comparator 110, whereas a voltage V_{BG}, illustratively from a bandgap reference, is provided to the non-inverting input 111. The comparator output is a binary value that is either high or low depending on whether the voltage on input 111 is greater or less then the voltage V_R on node 102. The comparator output is supplied on line 112 to control logic 113. The control logic includes a state machine that performs as a successive approximation register for controlling the outputs BIT0, BIT1, and BIT2 on lines 115, 116 and 117, respectively. The state machine is stepped through a sequence of states under the control of a clock provided on line 114, as more fully explained below.

Switches 107, 108 and 109 are placed across calibration resistors 103, 104 and 105, respectively. Each of the switches when closed forms a relatively low-impedance path around the corresponding resistor, being then effectively a short that produces approximately a zero voltage drop. Each switch when open has a relatively high impedance, providing for a voltage drop across the corresponding resistor according to its resistance value. The total voltage drop across the resistor string is the voltage V_R at node 102 with respect to ground (V_{SS}). It can be seen that $V_R = I_{REF} * R_{SUM}$, where R_{SUM} is the effective resistance of the resistor string, being the sum of the resistor values whose corresponding switches are open. Each switch is controlled by the corresponding output (BIT0, BIT1 or BIT2) of the state machine/successive approximation register 113.

Burger at col. 2, lines 8-42. To the Applicant's understanding, the passage fails to discuss a noise content of a reference output current and its relative value to a noise content of a reference voltage. Nothing in the passage appears to relate to relative noise values, inherently or otherwise. In fact, the word "noise" does not appear in that passage or any other part of Burger. Accordingly, the Applicant respectfully submits that the Office Action improperly asserts that "a noise content of the reference output voltage is inherently lower than a noise content of the reference voltage." If the Office still believes that relative noise values are somehow inherent in Burger's teachings, the Applicant respectfully requests production of concrete evidence to that effect (for example, an Examiner's declaration).

Because of at least the above reasons, the Office Action fails to set forth a proper *prima facie* obviousness rejection of claim 27. Furthermore, the Applicant submits that the Office Action fails to properly reject the rest of the pending claims, i.e., claims 28-51. Because claims 28-51 depend ultimately on claim 27, the Office Action may not base a proper obviousness rejection of those claims on Pangal and Burger. As described above, Pangal and Burger fail to teach or suggest at least some of the limitations of claim 27. Pangal and Burger therefore fail to render obvious any of the pending claims.

Because of at least the reasons described above, the Applicant respectfully submits that the presently pending claims are allowable over the cited references. The Applicant therefore respectfully requests a prompt Notice of Allowance.

CONCLUSION

The Applicant submits that the claims are in condition for allowance, and requests reconsideration of the application and a prompt Notice of Allowability. Furthermore, the Applicant believes that no fees are due in connection with this paper. Should any fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, however, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/SILA:095.

The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,

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